P3A4GL4BLF-GJN

Programmable Functions

- **Output Driver Impedance (34/48)**
- **CAS Write Latency (9/10/11/12/14/16/18)**
- **Additive Latency (0/CL-1/CL-2)**
- **$\overline{CS}$ to Command Address Latency (3/4/5/6/8)**
- **Command Address Parity Latency (4/5)**
- **Write Recovery Time (10/12/14/16/18/20/24)**
- **Burst Type (Sequential/Interleaved)**
- **RTT_PARK (34/40/48/60/80/120/240)**
- **RTT_NOM (34/40/48/60/80/120/240)**
- **RTT_WR (80/120/240)**
- **Read Preamble (1T/2T)**
- **Write Preamble (1T/2T)**
- **LPASR (Manual: Normal/Reduced/Extended, Auto:TS)**

Options

- **Package information**

  Lead-free RoHS compliance and Halogen-free

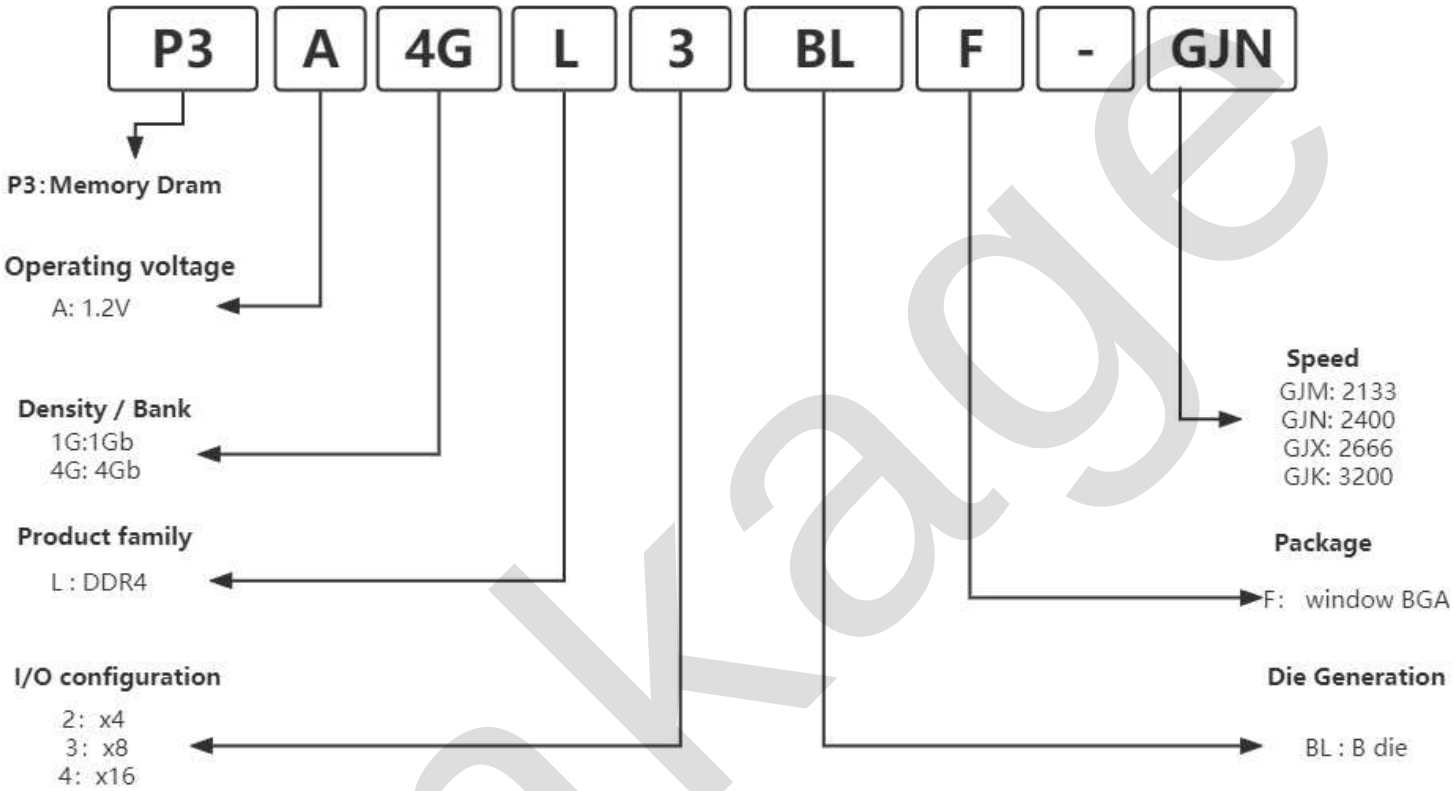
TFBGA Package	Dimension (mm)	Ball pitch (mm)
96-Ball	7.50 x 13.00	0.80

- **Temperature Range (T_c) [5]**
  - Commercial Grade : 0℃~95℃
  - Industrial Grade (-I) : -40℃~95℃
  - Quasi Industrial Grade (-T) : -40℃~95℃
- **VDD/VDDQ/VPP**
  - 1.2V / 1.2V / 2.5V

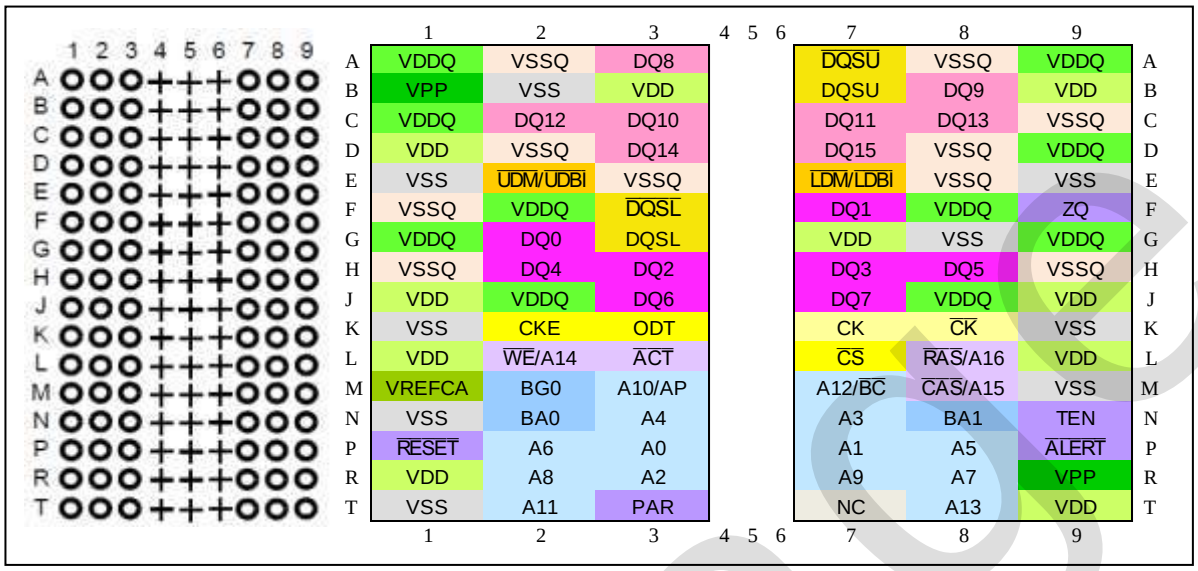
NOTE 1 Write Leveling feedback should be given on all data bits in parallel.
NOTE 2 For the same organization and voltage, the timing specification of high speed bin is backward compatible with low speed bin.
NOTE 3 Violating tREFI is not guaranteed.
NOTE 4 Violating tRFC is not guaranteed.
NOTE 5 When operate above 95℃, AC/DC will be derated.

Ordering Information

4Gb DDR4 ordering information table

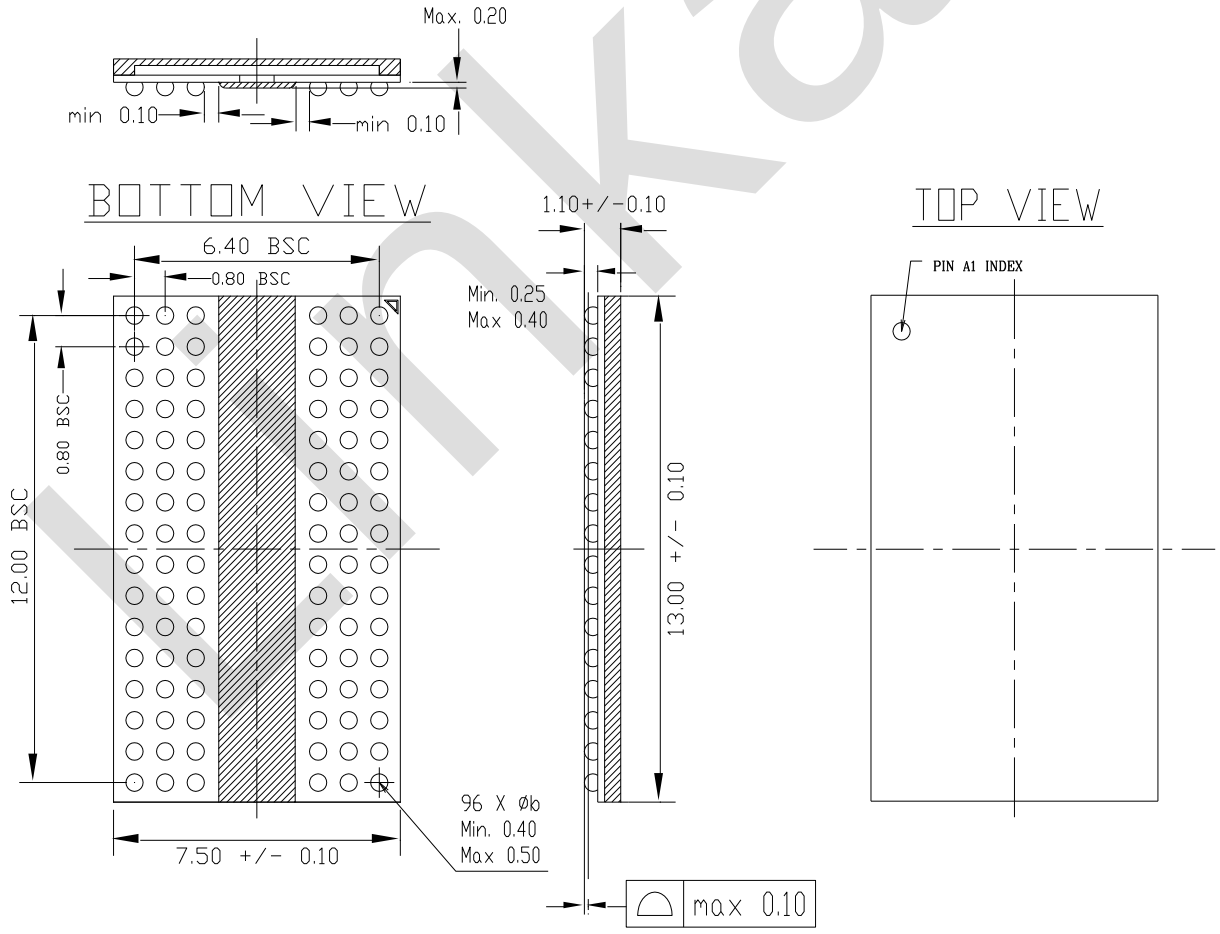


96 Ball TFBGA Package (X16)



	1	2	3	4 5 6	7	8	9	
A	VDDQ	VSSQ	DQ8		$\overline{DQSU}$	VSSQ	VDDQ	A
B	VPP	VSS	VDD		DQSU	DQ9	VDD	B
C	VDDQ	DQ12	DQ10		DQ11	DQ13	VSSQ	C
D	VDD	VSSQ	DQ14		DQ15	VSSQ	VDDQ	D
E	VSS	$\overline{UDM}$/UDBI	VSSQ		$\overline{LDM}$/LDBI	VSSQ	VSS	E
F	VSSQ	VDDQ	$\overline{DQSL}$		DQ1	VDDQ	ZQ	F
G	VDDQ	DQ0	DQSL		VDD	VSS	VDDQ	G
H	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ	H
J	VDD	VDDQ	DQ6		DQ7	VDDQ	VDD	J
K	VSS	CKE	ODT		CK	$\overline{CK}$	VSS	K
L	VDD	$\overline{WE}$/A14	$\overline{ACT}$		$\overline{CS}$	$\overline{RAS}$/A16	VDD	L
M	VREFCA	BG0	A10/AP		A12/$\overline{BC}$	$\overline{CAS}$/A15	VSS	M
N	VSS	BA0	A4		A3	BA1	TEN	N
P	$\overline{RESET}$	A6	A0		A1	A5	$\overline{ALERT}$	P
R	VDD	A8	A2		A9	A7	VPP	R
T	VSS	A11	PAR		NC	A13	VDD	T
	1	2	3	4 5 6	7	8	9	

Packge Outline Drawing



Ball Descriptions

Symbol	Type	Description
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (RTT) is applied only to each DQ, DQS, $\overline{DQS}$, $\overline{DM}$/$\overline{DBI}$/TDQS, configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
BA[1:0]	Input	**Bank Address Inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MRS cycle.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. BG1 but X16 has only BG0.
$\overline{ACT}$	Input	**Command input:** $\overline{ACT}$ defines the Activation command being entered along with $\overline{CS}$. The input into $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 will be considered as Row Address A16, A15 and A14
$\overline{RAS}$/A16 $\overline{CAS}$/A15 $\overline{WE}$/A14	Input	**Command Inputs:** $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 (along with $\overline{CS}$) define the command being entered. Those pins have multi-function. For example, for activation with $\overline{ACT}$ Low, those are Addressing like A16,A15 and A14 but for non-activation command with $\overline{ACT}$ High, those are Command pins for Read, Write and other command defined in command truth table.
A10/AP	Input	**Auto precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/$\overline{BC}$	Input	**Burst Chop:** Burst chop: A12/$\overline{BC}$ is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst-chopped).
For x4, A[16:0] For x8,x16 A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/$\overline{BC}$, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16, have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb.

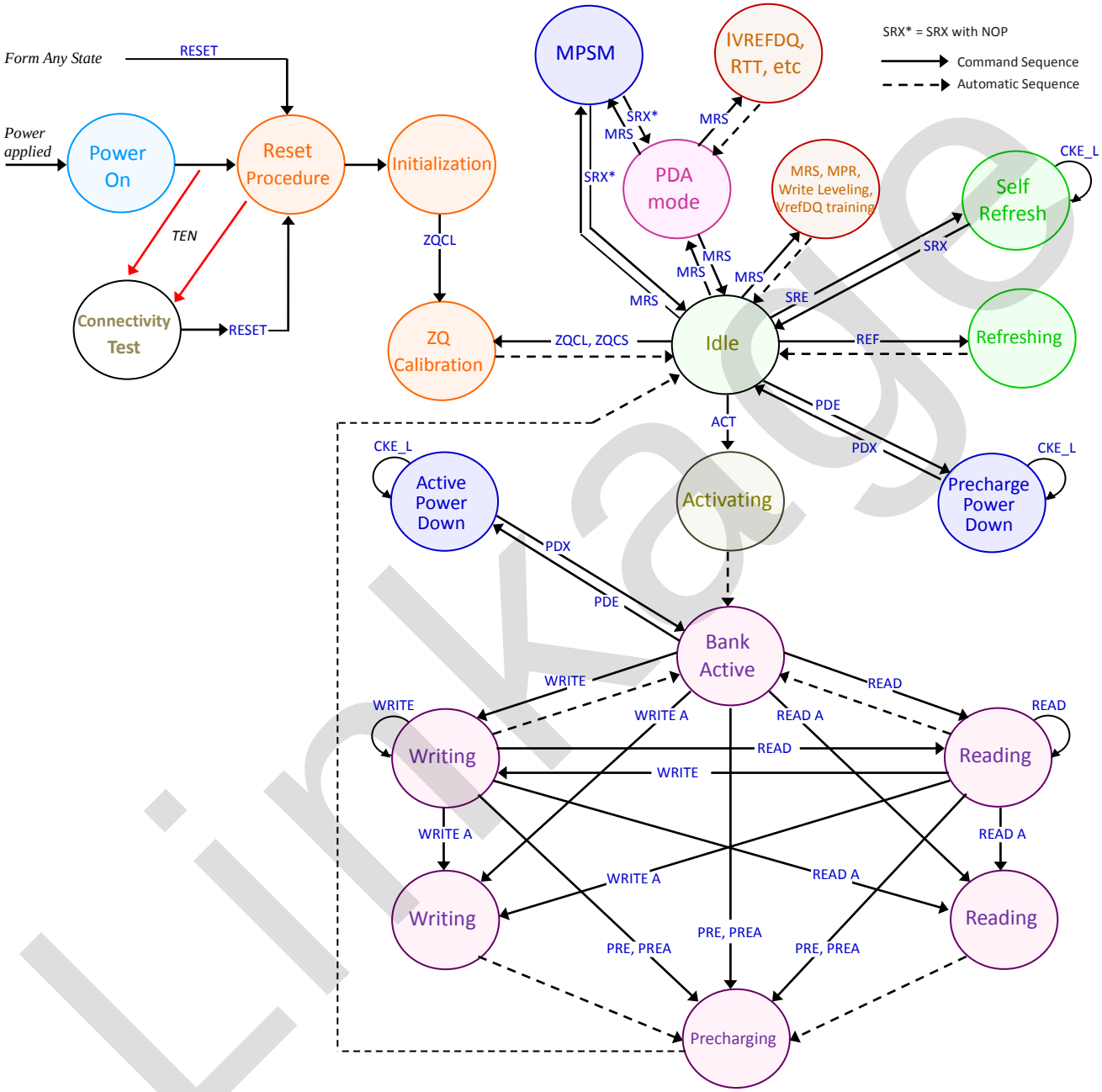
Symbol	Type	Description
PAR	Input	**Parity for command and address:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{ACT}$,$\overline{RAS}$/A16,$\overline{CAS}$/A15,$\overline{WE}$/A14, A12/$\overline{BC}$,A10/AP, A17-A0, BA0-BA1, BG0-BG1 Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and when $\overline{CS}$ is low.
DQ	Input/output	**Data input/output:** Bidirectional data bus. DQ represents DQ [3:0], DQ [7:0], and DQ [15:0] for the x16 configurations, respectively. If Write CRC is enabled via Mode register, then the Write CRC code is added at the end of Data Burst. Either anyone or all DQ0, DQ1, DQ2, and DQ3 is used as monitoring of internal Vref level during test via Mode Register Setting MR4 A4=High, training times change when enabled. During this mode, RTT value should be set to Hi-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS/$\overline{DQS}$ DQSL/$\overline{DQSL}$ DQSU/$\overline{DQSU}$	Input/output	**Data Strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, DQSL corresponds to the data on DQ [7:0]; DQSU corresponds to the data on DQ [15:8]. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
TDQS/$\overline{TDQS}$	Output	**Termination Data Strobe:** TDQS/$\overline{TDQS}$ is applicable for X8 DRAMs only. The TDQS function must be disabled in the mode register for x16 configurations. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same R_{TT} termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When the TDQS function is disabled via the mode register, the $\overline{DM}$/$\overline{DBI}$/ TDQS pin will provide the data mask ($\overline{DM}$) function or Data Bus Inversion ($\overline{DBI}$) depending on MR5, and the $\overline{TDQS}$ pin is not used.
$\overline{DM}$ $\overline{LDM}$, $\overline{UDM}$	Input	**Input data mask:** $\overline{DM}$ is an input mask signal for write data. Input data is masked when $\overline{DM}$ is sampled LOW coincident with that input data during a write access. $\overline{DM}$ is sampled on both edges of DQS. $\overline{DM}$ is muxed with $\overline{DBI}$ function by Mode Register A [12:10] setting in MR5. For x8 device, the function of $\overline{DM}$ or TDQS is enabled by Mode Register A11 setting in MR1. $\overline{DBI}$ is an input/output identifying whether to store/output the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if $\overline{DBI}$ is HIGH.
$\overline{DBI}$ $\overline{UDBI}$, $\overline{LDBI}$	Input/output	**DBI input/output:** Data bus inversion. $\overline{DBI}$ is an input/output signal used for data bus inversion in the x8 configuration. $\overline{UDBI}$ and $\overline{LDBI}$ are used in the x16 configuration; $\overline{UDBI}$ is associated with DQ [15:8], and $\overline{LDBI}$ is associated with DQ [7:0]. configurations. $\overline{DBI}$ can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See Data Bus Inversion (DBI).
$\overline{ALERT}$	Output	**Alert output:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then $\overline{ALERT}$ goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then $\overline{ALERT}$ goes LOW for relatively long period until ongoing DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, open-drain $\overline{ALERT}$ Pin must be bounded to VDD on board.
TEN	Input	**Connectivity test mode:** Connectivity Test Mode is active when TEN is HIGH, and inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
ZQ	Reference	**Reference pin for ZQ calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 0.96V for DC high and 0.24V for DC low.

Symbol	Type	Description
VPP	Supply	**DRAM activating power supply:** 2.5V (2.375V min , 2.75V max)
VDD	Supply	**Power Supply:** 1.2V ± 0.06V
VDDQ	Supply	**DQ Power Supply:** 1.2V ± 0.06V
VSS	Supply	**Ground**
VSSQ	Supply	**DQ Ground**
VREFCA	Supply	**Reference voltage for CA**
NC	-	**No Connect:** No internal electrical connection is present.
NF	-	**No function:** May have internal connection present, but has no function.
RFU	-	Reserved for future use.

NOTE Input only pins (BG0-BG1, BA0-BA1, A0-A17, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination.

Functional Description

Simplified State Diagram



Abbr.	Function	Abbr.	Function	Abbr.	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
RESET	Start RESET Procedure	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
ZQCS	ZQ Calibration Short	TEN	Boundary Scan Mode Enable	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	REF	Refresh, Fine granularity Refresh	MRS	Mode Register Set

RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings are defined:

Default MR settings for power-up and reset initialization

MR functions	MR bits	Value
Gear-down mode	MR3 A[3]=0	1/2 Rate
Per DRAM Addressability	MR3 A[4]=0	Disable
Max Power Saving Mode	MR4 A[1]=0	Disable
$\overline{CS}$ to Command/Address Latency	MR4 A[8:6]=000	Disable
CA Parity Latency Mode	MR5 A[2:0]=000	Disable
Hard Post Package Repair Mode	MR4 A[13]=0	Disable
Soft Post Package Repair Mode	MR4 A[5]=0	Disable

Power-Up and Initialization Sequence

The following sequence (Step 1-15) is required for power-up and initialization:

1) Apply power ($\overline{RESET}$ and TEN are recommended to be maintained below 0.2 × VDD; all other inputs may be undefined). $\overline{RESET}$ needs to be maintained below 0.2 x VDD for minimum 200µs with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700µs with stable power. CKE is pulled "LOW" any time before $\overline{RESET}$ is being deasserted (MIN time 10ns). The power voltage ramp time between 300mV to VDD min must be no greater than 200ms, and during the ramp, VDD ≥ VDDQ and (VDD-VDDQ) < 0.3Volts. VPP must ramp at the same time or earlier than VDD, and VPP must be equal to or higher than VDD at all times.

   During power-up, either of the following conditions may exist and must be met:

   • Condition A
   – VDD and VDDQ are driven from a single-power converter output, AND
   – The voltage levels on all balls other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
   – VTT is limited to 0.76V MAX when the power ramp is finished, AND
   – VREFCA tracks VDD/2.

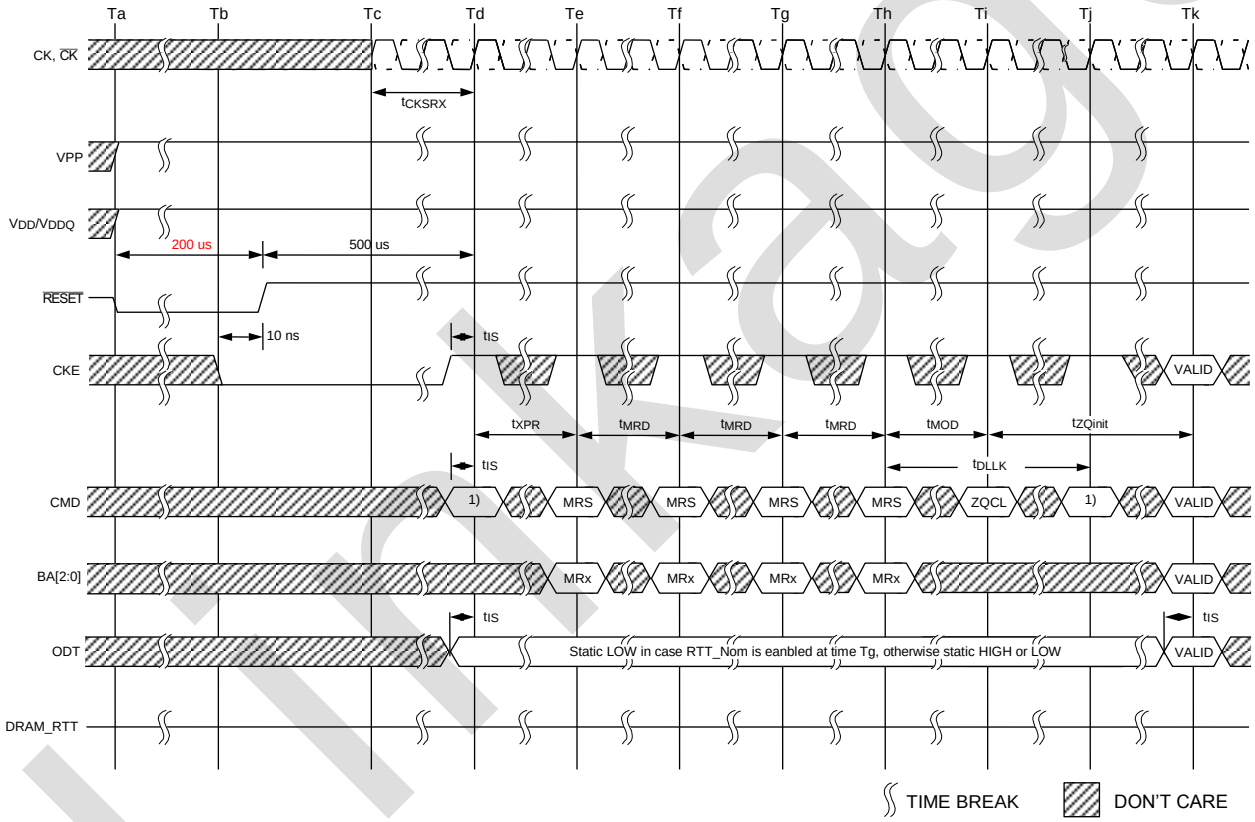
   • Condition B
   – Apply VDD without any slope reversal before or at the same time as VDDQ.
   – Apply VDDQ without any slope reversal before or at the same time as VTT and VREFCA.
   – Apply VPP without any slope reversal before or at the same time as VDD.
   – The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2) After $\overline{RESET}$ is de-asserted, wait for another 500µs until CKE becomes active.
   During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3) Clocks (CK, $\overline{CK}$) need to be started and stabilized for at least 10ns or 5 tCK (whichever is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a DESELECT command must be registered (with tIS setup time to clock) at clock edge Td. Once the CKE is registered "HIGH" after RESET, CKE needs to be continuously registered "HIGH" until the initialization sequence is finished, including expiration of tDLLK and tZQINIT.
4) The DDR4 SDRAM keeps its ODT in High-Impedance state as long as $\overline{RESET}$ is asserted. Further, the SDRAM keeps its ODT in High-Impedance state after $\overline{RESET}$ deassertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is

finished, including the expiration of tDLLK and tZQINIT.

5) After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, tXPR, before issuing the first MRS command to load mode register (tXPR = MAX (tXS; 5 × tCK).
6) Issue MRS command to load MR3 with all application settings, wait tMRD.
7) Issue MRS command to load MR6 with all application settings, wait tMRD.
8) Issue MRS command to load MR5 with all application settings, wait tMRD.
9) Issue MRS command to load MR4 with all application settings, wait tMRD.
10) Issue MRS command to load MR2 with all application settings, wait tMRD.
11) Issue MRS command to load MR1 with all application settings, wait tMRD.
12) Issue MRS command to load MR0 with all application settings, wait tMOD.
13) Issue a ZQCL command to starting ZQ calibration.
14) Wait for both tDLLK and tZQINIT completed.
15) The DDR4 SDRAM is now ready for read/write training (include Vref training and Write leveling).

RESET and Initialization Sequence at Power-On Ramping



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

VDD Slew rate at Power-up Initialization Sequence

VDD Slew Rate

Symbol	Min	Max	Units	NOTE
VDD_sl	0.004	600	V/ms	1,2
VDD_ona		200	ms	3

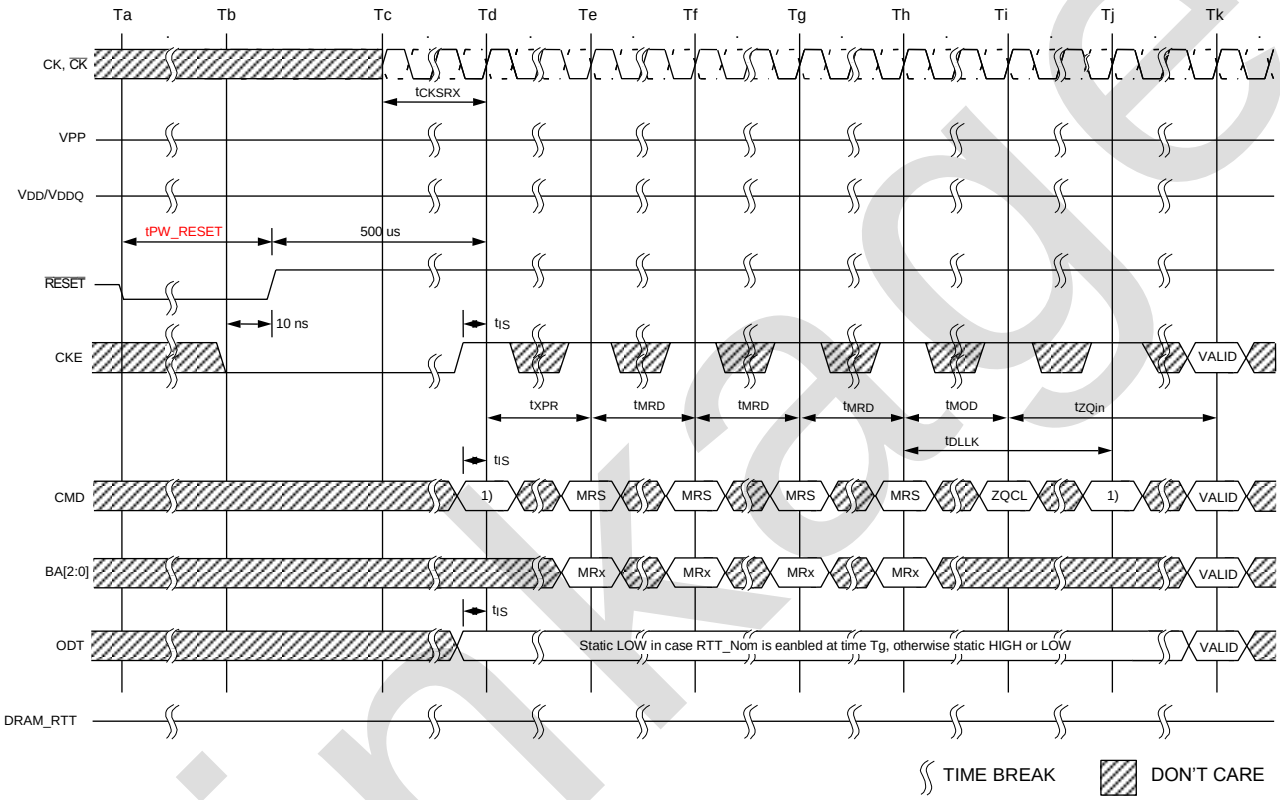
NOTE 1 Measurement made between 300mV and 80% VDD minimum.
NOTE 2 20 MHz bandlimited measurement
NOTE 3 Maximum time to ramp VDD from 300 mV to VDD minimum.

RESET Initialization with Stable Power Sequence

The following sequence is required for $\overline{\text{RESET}}$ at no power interruption initialization:

1. Assert $\overline{\text{RESET}}$ below 0.2 × VDD anytime when reset is needed (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum tPW_RESET. CKE is pulled LOW before $\overline{\text{RESET}}$ being de-asserted (MIN time 10ns).
2. Follow Steps 2 to 10 in the Reset and Initialization Sequence at Power-on Ramping procedure.
3. The reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include Vref training and Write leveling)

RESET Procedure at Power Stable



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

Register Definition

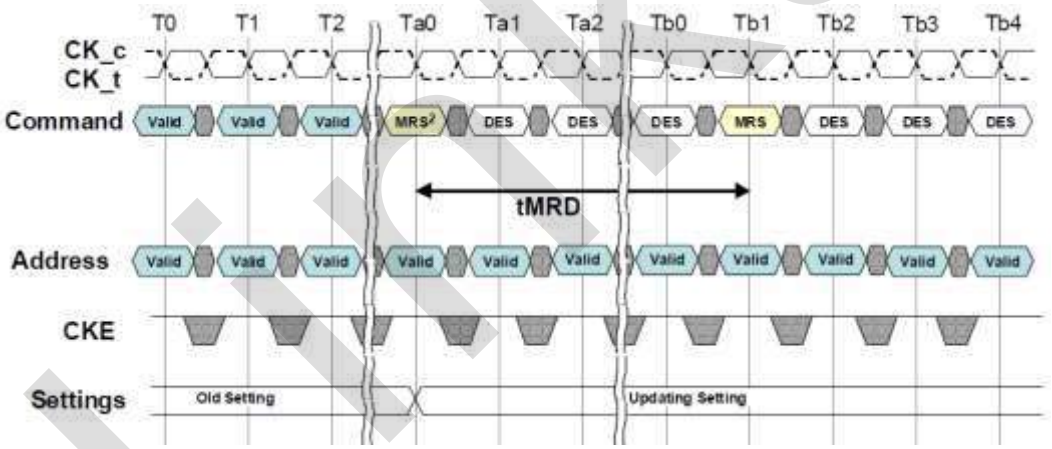
Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

tMRD Timing

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

The MRS commands which do not apply tMRD timing to next MRS command are listed in note 2 of the following figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

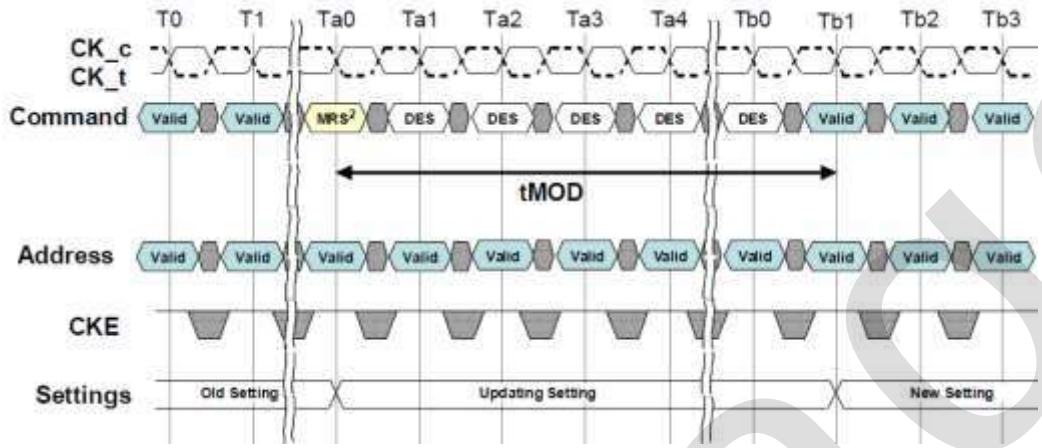
NOTE 2 tMRD applies to all MRS commands with the following exceptions:

- Geardown Mode
- C/A Parity Latency Mode
- CS to Command/Address Latency Mode
- Per DRAM Addressability Mode
- VrefDQ training value, VrefDQ training mode, and VrefDQ Training Range

tMOD Timing

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET, and is the minimum time required from an MRS command to a nonMRS command, excluding DES.

Some of the mode register setting cases, function updating takes longer than tMOD. The MRS commands which do not apply tMOD timing to next valid command excluding DES is listed in note 2 of the following figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



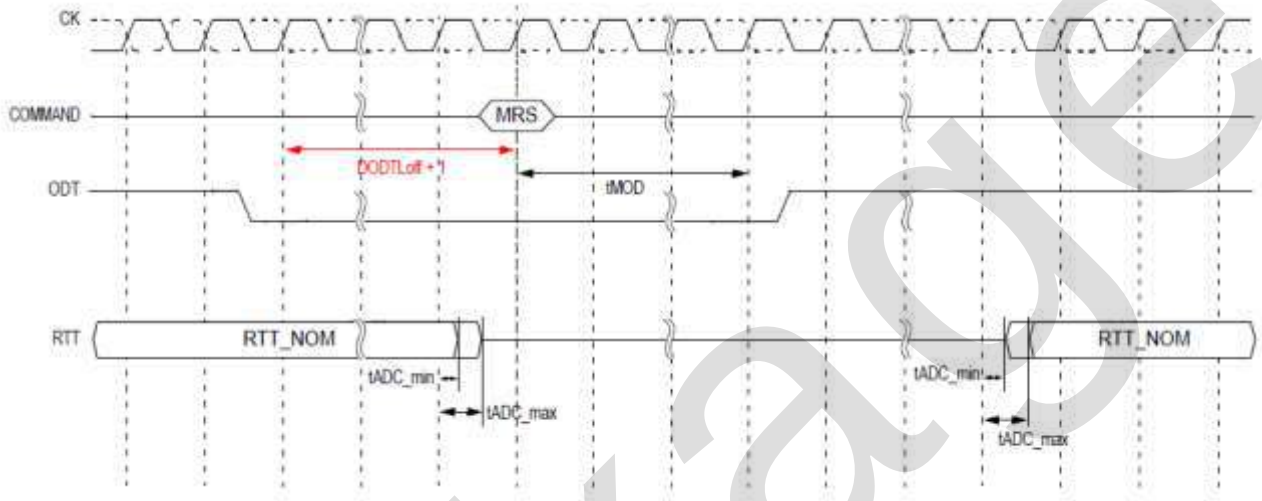
NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

NOTE 2 List of MRS commands exception that do not apply to tMOD.

- DLL Enable, DLL Reset
- VrefDQ training value, internal Vref monitor, VrefDQ training mode, and VrefDQ Training Range
- Geardown Mode
- Per DRAM Addressability Mode
- Maximum Power Saving Mode
- CA Parity Mode

ODT Status at MRS affecting ODT turn-on/off timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of the following figure for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don't care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.



NOTE 1 This timing diagram shows CA Parity Latency mode is "Disable" case.

NOTE 2 When an MRS command mentioned in this note affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value, this means the MR register value changes. The ODT signal should set to be low for at least DODTLoff +1 clock before their affecting MRS command is issued and remain low until tMOD expires. The following MR registers affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value and it requires ODT to be low when an MRS command change the MR register value. If there are no change the MR register value that correspond to commands mentioned in this note, then ODT signal is not require to be low.

- DLL control for precharge power down
- Additive latency and CAS read latency
- DLL enable and disable
- CAS write latency
- CA Parity mode
- Gear Down mode
- RTT_NOM

Mode Register

MR0

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	BG0 / BA1 / BA0 / MR Select **0 / 0 / 0 / MR0** 0 / 0 / 1 / MR1 0 / 1 / 0 / MR2 0 / 1 / 1 / MR3 1 / 0 / 0 / MR4 1 / 0 / 1 / MR5 1 / 1 / 0 / MR6 1 / 1 / 1 / RCW[1]
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13][5], A[11:9]	WR and RTP[2,3]	See table: Write Recovery and Read to Precharge
A[8]	DLL Reset	0 = No 1 = Yes
A[7]	TM	0 = Normal 1 = Test
A[12, 6:4, 2]	CAS Latency[4]	See Table: CAS Latency
A[3]	Read Burst Type	0 = Sequential 1 = Interleave
A[1:0]	Burst Length	00 = 8 (Fixed) Abbreviated BL8 01 = BC4 or 8 (on the fly) Abbreviated BC4OTF or BL8OTF 10 = BC4 (Fixed) Abbreviated BC4 11 = Reserved

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 WR (write recovery for autoprecharge) min in clock cycles is calculated by following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

NOTE 3 The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

NOTE 4 The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to speed bin tables for each frequency. CAS Latency controlled by A12 is optional for 4Gb device.

NOTE 5 A13 for WR and RTP setting is optional for 4Gb.

Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	RFU	RFU
1	0	1	0	RFU	RFU
1	0	1	1	RFU	RFU
1	1	0	0	RFU	RFU
1	1	0	1	RFU	RFU
1	1	1	0	RFU	RFU
1	1	1	1	RFU	RFU

CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	Reserved
0	0	0	0	1	Reserved
0	0	0	1	0	**11**
0	0	0	1	1	**12**
0	0	1	0	0	**13**
0	0	1	0	1	**14**
0	0	1	1	0	**15**
0	0	1	1	1	16
0	1	0	0	0	**18**(1)
0	1	0	0	1	**20**(1)
0	1	0	1	0	**22**(1)
0	1	0	1	1	**24**(1)
0	1	1	0	0	Reserved
0	1	1	0	1	**17**
0	1	1	1	0	**19**
0	1	1	1	1	**21**
1	0	0	0	0	**25**(1)
1	0	0	0	1	Reserved
1	0	0	1	0	Reserved
1	0	0	1	1	Reserved
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved

Note 1: this CL setting is related to read DBI usage only and please check “Speed bin” section and have a proper corresponding option to use.

MR1

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[3]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12]	Qoff[1]	0 = Output buffer enable 1 = Output buffer disable
A[11]	TDQS enable	0 = Disable 1 = Enable
A[10:8]	RTT_NOM	See Table: RTT_NOM
A[7]	Write Leveling Enable	0 = Disable 1 = Enable
A[6:5]	RFU	0 = must be programmed to 0 during MRS
A[4:3]	Additive Latency	00 = 0 (AL disabled) 01 = CL-1 10 = CL-2 11 = Reserved
A[2:1]	Output Driver Impedance Control	See Table: Output Driver Impedance Control
A[0]	DLL Enable	0 = Disable[2] 1 = Enable

NOTE 1 Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s.

NOTE 2 States reversed to “0 as Disable” with respect to DDR4.

NOTE 3 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	Disabled
0	0	1	RZQ/4 (60 Ω)
0	1	0	RZQ/2 (120 Ω)
0	1	1	RZQ/6 (40 Ω)
1	0	0	RZQ/1 (240 Ω)
1	0	1	RZQ/5 (48 Ω)
1	1	0	RZQ/3 (80 Ω)
1	1	1	RZQ/7 (34 Ω)

Output Driver Impedance Control

A2	A1	ODI
0	0	RZQ/7(34 ohm)
0	1	RZQ/5(48 ohm)
1	0	RFU
1	1	RFU

MR2

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12]	Write_CRC	0 = Disable 1 = Enable
A[11:9]	RTT_WR	See Table: RTT_WR
A[8]	RFU	0 = must be programmed to 0 during MRS
A[7:6]	Low Power Auto Self Refresh (LPASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A[5:3]	CAS Write Latency(CWL)	See Table: CWL (CAS Write Latency)
A[2:0]	RFU	0 = must be programmed to 0 during MRS

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

CAS Write Latency (CWL)

A5	A4	A3	CWL	Speed Grade in MT/s			
				1 tCK tWPRE		2 tCK tWPRE[1]	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	2933	2400	2666	2400
1	1	0	18	-	2666	2933	2666
1	1	1	20	-	2933	-	2933

NOTE 1 The 2 tCK Write Preamble is valid for DDR4-2400/2666/2933 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

MR3

<table>
<tr><th>Address</th><th>Operating Mode</th><th>Description</th></tr>
<tr><td>BG[1]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>BG[0], BA[1:0]</td><td>MR Select</td><td>
<table>
<tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr>
</table>
</td></tr>
<tr><td>A[17]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[13]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[12:11]</td><td>MPR Read Format</td><td>00 = Serial
01 = Parallel
10 = Staggered
11 = Reserved</td></tr>
<tr><td>A[10:9]</td><td>Write CMD Latency
when CRC and DM are enabled</td><td>See Table:
Write Command Latency when CRC and DM are both enabled</td></tr>
<tr><td>A[8:6]</td><td>Fine Granularity Refresh Mode</td><td>See Table: Fine Granularity Refresh Mode</td></tr>
<tr><td>A[5]</td><td>Temperature sensor readout[2]</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[4]</td><td>Per DRAM Addressability</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[3]</td><td>Geardown Mode</td><td>0 = 1/2 Rate
1 = 1/4 Rate</td></tr>
<tr><td>A[2]</td><td>MPR Operation</td><td>0 = Normal
1 = Dataflow from/to MPR</td></tr>
<tr><td>A[1:0]</td><td>MPR Page Selection</td><td>00 = Page0
01 = Page1
10 = Page2
11 = Page3
See Table: MPR Data Format</td></tr>
</table>

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 Please confirm with NTC.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh Mode
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	RFU
1	0	0	RFU
1	0	1	Enable On-the-fly 1x/2x
1	1	0	Enable On-the-fly 1x/4x
1	1	1	RFU

MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write CMD Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866/2133/2400/2666
1	0	6nCK	2933
1	1	RFU	RFU

NOTE 1 Write Command latency when CRC and DM are both enabled
NOTE 2 At less than or equal to 1600 then 4nCK; neither 5nCK nor 6nCK
NOTE 3 At greater than 1600 and less than or equal to 2666 then 5nCK; neither 4nCK nor 6nCK

MPR Data Format

MR3 MPR Page A[1:0]	Purpose	MPR Location BA[1:0]	MPR Bit Write Location [7:0]								Note
			7	6	5	4	3	2	1	0	
			Read Burst Order (serial mode)								
			UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7	
00 Page 0	Training Patterns	**00** = MPR0	0	1	0	1	0	1	0	1	1,2
		01 = MPR1	0	0	1	1	0	0	1	1	
		10 = MPR2	0	0	0	0	1	1	1	1	
		11 = MPR3	0	0	0	0	0	0	0	0	
01 Page 1	C/A Parity Error Log	**00** = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	3,4,5,6
		01 = MPR1	$\overline{CAS}$/A15	$\overline{WE}$/A14	A13	A12	A11	A10	A9	A8	
		10 = MPR2	PAR	$\overline{ACT}$	BG1	BG0	BA1	BA0	A17[6]	$\overline{RAS}$/A16	
		11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[6]			-	-	-	
					MR5	MR5	MR5				
					A2	A1	A0				
10 Page 2	MRS Readout	**00** = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status[8]		CRC Write Enable	R_{TT}_WR		
			-	-	MR2	Refer to next table		MR2	MR2		
			-	-	A11			A12	A10	A9	
		01 = MPR1	Vref DQ range	Vref DQ training Value						Geardown Enable	
			MR6	MR6						MR3	
			A6	A5	A4	A3	A2	A1	A0	A3	
		10 = MPR2	CAS Latency					CAS Write Latency			
			MR0					MR2			
			A6	A5	A4	A2	A12	A5	A4	A3	
		11 = MPR3	R_{TT}_NOM			R_{TT}_PARK			Driver Impedance		
			MR1			MR5			MR1		
			A10	A9	A6	A8	A7	A6	A2	A1	
11 Page 3	Vendor use only[7]	**00** = MPR0	Don't care								7
		01 = MPR1	Don't care								
		10 = MPR2	Don't care								
		11 = MPR3	Don't care								

NOTE 1 MPRx using A7:A0 that A7 is mapped to location [7] and A0 is mapped to location [0].
NOTE 2 Training pattern be defined by MPR0-MPR3 which are default value of Page 0 read and write
NOTE 3 MPR used for C/A parity error log readout is enabled by setting A [2] in MR3
NOTE 4 For higher density of DRAM, where A [17] is not used, MPR2[1] should be treated as don't care.
NOTE 5 If a device is used in monolithic application, where C [2:0] are not used, then MPR3[2:0] should be treated as don't care.
NOTE 6 MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.
NOTE 7 MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.
NOTE 8 Please confirm with NTC.

Temperature Sensor Status

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range	MR3[5]
0	0	Sub 1x refresh (>tREFI)	**MR3 bit A5=1 (Temperature sensor readout = Enabled)** DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A [4:3]). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits. **MR3 bit A5=0 (Temperature sensor readout = Disabled)** DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A[4:3])
0	1	1x refresh rate (= tREFI)	
1	0	2x refresh rate (1/2 x tREFI)	
1	1	RFU	

MR4

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	hPPR	0 = Disable 1 = Enable
A[12]	Write Preamble	0 = 1 nCK 1 = 2 nCK
A[11]	Read Preamble	0 = 1 nCK 1 = 2 nCK
A[10]	Read Preamble Taring Mode	0 = Disable 1 = Enable
A[9]	Self Refresh Abort	0 = Disable 1 = Enable
A[8:6]	CS to CMD/ADDR Latency Mode (Cycles)	See Table: CS to CMD/ADDR Latency Mode Setting
A[5]	sPPR	0 = Disable 1 = Enable
A[4]	Internal Vref Monitor	0 = Disable 1 = Enable
A[3]	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A[2]	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A[1]	Maximum Power Down Mode	0 = Disable 1 = Enable
A[0]	RFU	0 = must be programmed to 0 during MRS

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disabled
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

<table>
<tr><th>Address</th><th>Operating Mode</th><th>Description</th></tr>
<tr><td>BG[1]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>BG[0], BA[1:0]</td><td>MR Select</td><td>
<table>
<tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr>
</table>
</td></tr>
<tr><td>A[17]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[13]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[12]</td><td>Read DBI</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[11]</td><td>Write DBI</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[10]</td><td>Data Mask</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[9]</td><td>CA Parity Persistent Error</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[8:6]</td><td>RTT_PARK</td><td>See Table: RTT_PARK</td></tr>
<tr><td>A[5]</td><td>ODT Input Buffer during Power Down Mode</td><td>0 = ODT input buffer is activated
1 = ODT input buffer is deactivated</td></tr>
<tr><td>A[4]</td><td>C/A Parity Error Status</td><td>0 = Clear
1 = Error</td></tr>
<tr><td>A[3]</td><td>CRC Error Clear</td><td>0 = Clear
1 = Error</td></tr>
<tr><td>A[2:0]</td><td>C/A Parity Latency Mode</td><td>See Table: C/A Parity Latency Mode</td></tr>
</table>

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A2	A1	A0	CA Parity Latency	Speed Bin
0	0	0	Disabled	
0	0	1	4	1600/1866/2133
0	1	0	5	2400/2666
0	1	1	6	2933
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTE 1 Parity latency must be programmed according to timing parameters by speed grade table.